WHAT IS CLAIMED:

1. A timing control device for the compensation of timing errors in multple channel devices comprising at least one register, the device comprising:

a clock for providing a clock signal;

a reference signal generator for providing a reference signal applicable through a reference channel to said register, for deskewing the register's channels with respect to said reference signal;

wherein for each said register a corresponding feedback loop is associated for the relative alignment of register's channels timing in relation to the reference signal, said feedback loop comprising

a means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence of symbols transmitted through the reference channel; and

a set of delay means which uses the determined information on deviation from the predetermined level of said probability to generate a feedback signal to compensate timing errors in said register.

2. A timing control device according to claim 1 further comprising a sample hold device for holding a value of a first symbol in a sequence of repetitive signals transmitted through the reference channel.

3. A timing control device according to claim 1, further comprising a modulator signal applied to the reference signal for obviating the timing hysteresis within the register.

4. A timing control device according to claim 1, wherein the reference signal changes state once per a predefined number of clock cycles.

5. A timing control device according to claim 1, wherein the reference signal is the clock signal with a constant delay.

6. A timing control device according to claim 3, wherein the modulator signal is generated by the oscillation of a channel of the register or another register.

7. A timing control device according to claim 1, wherein the set of delay means comprises a variable delay which is an analogue delay element having a monotonic transfer function.

8. A timing control device according to claim 1, wherein the set of delay means comprises a variable delay which is a digital delay element having a monotonic transfer function.

9. A timing control device according to claim 1, wherein the detecting means comprises an integrator and/or an amplifier and/or a filter.

10. A timing control device according to claim 9, wherein the filter comprises a low pass filter to reduce the bandwidth of the feedback signal to within the range of the integrator.

11. A timing control device according to claim 1, wherein the feedback loop comprises digital components for the integrator.

12. A timing control device according to claim 1, wherein the feedback loop comprises analogue components to generate a continuously variable feedback signal.

13. A timing control device according to claim 1, further comprising a duty cycle correction means.

14. A timing control device according to claim 1, further comprising a means for correcting skew caused by differences in time of crossing the threshold.

15. A self calibrating receiver comprising:

a register having a plurality of channels having inputs and outputs;

a clock means for providing a clock signal to the register;

a reference signal generator connectable to the input of at least one said channel of said register for supplying reference signals for deskewing the register;

a detecting means connectable to the output of at least one said channel of said register for detecting a deviation from a predetermined level of probability of reading by said register from said reference channel a desired symbol on a boundary of two reference channel symbols in a sequence;

wherein the output of the detecting means is connectable to a set of delay means which uses the information received by said detecting means to generate a feedback signal to compensate timing errors in said register.

16. The self calibrating receiver according to claim 15, further comprising a sample hold device for holding a value of a first symbol in a sequence of repetitive signals transmitted through the reference channel.

17. The self calibrating receiver according to claim 15, wherein the reference signal changes state once per a predefined number of clock cycles.

18. The self calibrating receiver according to claim 15, wherein the reference signal is the clock to the register signal.

19. The self calibrating receiver according to claim 15, wherein the reference signal is delayed by a fixed delay preferably to centre the reference transition in the middle of the programmable range of the variable delay on the clock path.

20. The self calibrating receiver according to claim 15, wherein the detecting means comprises an integrator and/or an amplifier and/or a filter.

21. The self calibrating receiver according to claim 20, wherein the filter is a low pass filter for reducing the bandwidth of the feedback signal to within the range of the integrator.

22. The self calibrating receiver according to claim 15, further comprising a modulator signal applied to the reference signal for obviating the timing hysteresis within said register.

23. The self calibrating receiver according to claim 22, wherein the modulator signal is generated by the oscillation of a channel of the register or another register.

24. The self calibrating receiver according to claim 15, when used as a phase comparator.

25. The self calibrating receiver according to claim 15, when used as a plurality of phase comparators using the same reference clock.

26. A self calibrating transmitter with expandable data width, comprising:

at least one register having at least one channel having an input and output;

a clock means for providing a clock signal to said register;

a reference signal generator for supplying reference signals for deskewing said register's channel output in relation to the reference signal;

a phase comparator, one input of which is connected to the reference signal and another input is connected to a sense signal at the register's output; and

at least one feedback loop associated with the output of said phase comparator, the feedback loop comprising a set of delay means to compensate the timing errors in transmitter channels, wherein

the reference signal is connectable to the input of the phase comparator; and

an input of at least one said channel of said register is connectable to another signal for providing the sense signal to the phase comparator for deskewing the register.

27. The transmitter according to claim 26, wherein the register comprises a plurality of channels for data transmitting and/or providing sense signal to phase comparator for deskewing the register.

28. The self calibrating transmitter according to claim 26, wherein the phase comparator is a self calibrated receiver as claimed in claim 15.

29. The self calibrating transmitter according to claim 26, wherein the phase comparator is a flip-flop.

30. The self calibrating transmitter according to claim 26, further comprising a sample hold device for holding a value of a first symbol in a sequence of repetitive signals transmitted through the reference channel.

31. The self calibrating transmitter according to claim 26, wherein the reference signal changes state once per a predefined number of clock cycles.

32. The self calibrating transmitter according to claim 26, wherein the necessity for a plurality of channels is obviated by using a data channel where the data has known characteristics and control over the feedback system to ensure the data has transitions.

33. The self calibrating transmitter according to claim 32, wherein the input of at least one other channel of the self calibrating receiver is connected to other drivers for calibrating them in relation to the reference clock.

34. The self calibrating transmitter according to claims 26, further comprising a modulator signal applied to the reference signal for obviating the timing hysteresis within said register.

35. The self calibrating transmitter according to claim 26, wherein said transmitter reference signal is selected from non-inverted, inverted, and differential.

36. The transmitter according to claim 26, wherein said another signal for providing the sense signal to the phase comparator for deskewing the register is selected from single-ended reference, both single-ended and inverted reference, and differential reference signal.

37. The transmitter according to claim 26, wherein said phase comparator comprises at least one channel for providing rising edge sense signal and at least one channel for providing falling edge sense signal to phase comparators for deskewing the register.

38. The transmitter according to claim 37, wherein both the rising edge sense signal and the falling edge sense signal at the register's output are connected to said phase comparators.

39. The transmitter according to claim 38, wherein the rising edge sense signal is further connected to a second phase comparator for duty cycle correction.

40. An integrated circuit incorporating at least one register and a timing control device for the compensation of timing errors to create the characteristics of a zero setup and hold time integrated circuit, wherein

the timing control device comprises:

a clock for providing a clock signal;

a reference signal generator for providing a reference signal applicable through a reference channel to said register, for deskewing the register's channels with respect to said reference signal;

wherein for each said register a corresponding feedback loop is associated for the relative alignment of register's channels timing in relation to the reference signal, said feedback loop comprising

a means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence of symbols transmitted through the

reference channel; and

a set of delay means which uses the determined information on deviation from the predetermined level of said probability to generate a feedback signal to compensate timing errors in said register.

41. An interface for high speed data transmission, incorporating the timing control device according to claim 1.

42. A test system incorporating at least one register and a timing control device for the compensation of timing errors, wherein the timing control device comprises:

a clock for providing a clock signal;

a reference signal generator for providing a reference signal applicable through a reference channel to said register, for deskewing the register's channels with respect to said reference signal;

wherein for each said register a corresponding feedback loop is associated for the relative alignment of register's channels timing in relation to the reference signal, said feedback loop comprising

a means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence of symbols transmitted through the reference channel; and

a set of delay means which uses the determined information on deviation from the predetermined level of said probability to generate a feedback signal to compensate timing errors in said register.

43. A method for the compensation of timing errors in multiple channel devices comprising at least one register, the method comprising the steps of:

providing a clock signal to said register;

providing reference signals for deskewing the register;

providing reference signals for deskewing the register;

detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence; and

generating for each said register a feedback signal using the determined information on deviation to compensate timing errors in said register until the clock reaches a zero skew with respect to the reference signal.

44. A method according to claim 43, wherein the deviation is further treated using an integrator.

45. A method according to claim 43, wherein the deviation is further treated using an amplifier.

46. A method according to claim 43, further comprising a step of filtering, such as in a low pass filter, to reduce the bandwidth of the feedback signal to within the range of the integrator.

47. A method according to claim 43, further comprising a step of supplying a modulator signal applied to the reference signal for obviating the timing hysteresis within the register.

48. A method according to claim 47, wherein the modulator signal is generated by the oscillation of a channel of the register or another register.

49. A method according to claim 43, wherein the feedback signal is generated using the information determined either for rising, or falling edge.

50. A method according to claim 49, wherein both the rising and falling edges are levelled with respect to the reference clock.

51. A method according to claim 49, wherein even rising, even falling and odd rising edges are levelled with respect to the reference clock.